MOSFET Model Analysis for Submicron and Nanometer Bulk-driven Applications

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Abstract

Bulk-driven MOSFET technique meets the low-voltage and low-power requirements demanded in the modern analog circuit design. Due to submicron/nanometer technologies and critical short-channel effects, choosing a suitable MOSFET model for circuit design becomes increasingly important. However, the conventional MOSFET models normally set up for the typical gate-driven applications may not perform correctly and accurately for the bulk-driven applications in the advanced technologies. In this paper, three most widely used MOSFET models, including BSIM, EKV, and PSP, have been extracted for the modern technologies and used in the simulation of bulk-driven applications. Measurement data of fabricated devices are compared with simulation results from distinct models. Several critical MOSFET parameters have been chosen to compare and analyze MOSFET characteristics. The experimental results demonstrate the advantages of the bulk-driven technique compared with the gate-driven scheme. Finally, the performance of distinct MOSFET models is summarized in order to provide analog circuit designers with practical directives.

Keywords: Bulk-driven; MOSFET; Model; Submicron; Nanometer

1. Introduction

With the reduction in minimum dimension of MOSFET channel size in the advanced technologies, achieving lower power supplies has become a critical aspect in modern analog circuit design. The fundamental limitation of low-voltage circuit design using the existing design methodology is that the power supply must be at least equal to the sum of the magnitude of the cascode p-type and n-type threshold voltages. Thus, several possible techniques, such as bulk-driven, sub-threshold, self-cascode, and floating-gate, have been developed to construct high performance analog circuits under low power supply voltages.

The bulk-driven technique, which uses bulk terminal as signal input, is a promising method as it achieves enhanced performance without having to modify the existing structure of MOSFET [1]. For a traditional MOSFET, it is mandatory to meet the requirement of $V_{GS} > V_{th}$ in order to make the MOSFET function in the triode or saturation region. In contrast, the bulk-driven technique allows even smaller voltage to be set at the input terminal but still generate saturation voltage at the output [2]. When applying this technique in the circuit design, satisfactory performance especially in the low-voltage and low-power applications can be achieved.

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In recent years, bulk-driven technique has attracted strong interest from researchers. Most of them focus on building-block circuits such as current mirror [3], OTA [4], and mixer [5]. Furthermore, some prior work on the comparison of MOSFET models in the gate-driven applications shows one model tends to have advantages in the approximation of certain parameters but disadvantages in other applications [6][7]. To the best of our knowledge, thus far there is no systematic analysis on MOSFET models for bulk-driven circuit simulation. In this paper, we are motivated to evaluate the performance of distinct MOSFET models for bulk-driven applications in 0.18μm and 90nm technologies and compare measurement data with simulation results.

The paper is organized as follows. Section 2 discusses the bulk-driven technique and fundamental model analysis. Section 3 exhibits the comparison of measurement and simulation results followed by the performance evaluation. Finally, the conclusions are drawn in Section 4.

2. Background

2.1. Bulk-driven Technique

The principle of the bulk-driven technique is that the input voltage is greater than zero for NMOS and less than zero for PMOS so that the threshold voltage will be reduced accordingly. In addition, the bulk-driven configuration is able to provide the same level current by applying lower voltage to bulk terminal compared to the gate-driven scheme. To simulate and measure MOSFET performance in 0.18μm and 90nm technologies, in this paper, MOSFETs with the same channel size under the same configuration have been employed. For the gate-driven simulation, we sweep the gate-source input voltage and fix the voltages of the other three terminals. For the bulk-driven simulation, we sweep the bulk-source input voltage and fix the voltages of the other three terminals. As for PMOS, work need to substitute NMOS with PMOS and set voltage with negative value.

The measurement environment is built up with the aid of a semiconductor parameter analyzer and its test fixture. The measurement data for 0.18μm and 90nm technology are available in this paper. To remove random errors due to process, for each MOSFET device with specific channel size, we measured five chips and got their mean values. So in this paper, the measurement data used for comparison are statistical ones.

2.2. Analysis of Distinct MOSFET Models

In a traditional CMOS design, MOSFETs normally employ gate terminal as input of signals. However, when the channel lengths are much smaller than a micrometer, the gate-driven applications will cause operational problems. The fact is that the supply voltage reduces at a faster pace than the threshold voltage. One possible solution is to use the bulk-driven technique, which treats the bulk terminal as “a second gate”. The input voltage is set up between the bulk terminal and the source terminal. The basic concept of the bulk-driven technique is based on equation 1 below, which shows the body effect:

\[ V_{th} = V_{th0} + \gamma \left( \sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_p} \right) \]  

(1)

When the input voltage is under 1V, the bulk-driven MOSFET configuration can not only remove the requirement of VGS > VT, but also reduce the threshold voltage. And this technique allows small voltage less than 1V to be set at the input to generate the saturation voltage at the output [4]. When applying the
bulk-driven technique in the circuit design, we can achieve satisfactory performance especially in the low-voltage and low-power applications.

1) BSIM Model

Both BSIM3V3 and BSIM4 are popular BSIM models currently used in industry and academia. Focusing on gate-driven applications, the BSIM3V3 model achieves high performance in 0.18μm and above processes. In contrast, BSIM4 model pays more attention to 90nm or less process nodes. In this paper, the BSIM3V3 model based on 0.18μm technology has been chosen for submicron technology analysis. The BSIM4 models extracted from 90nm technology are used for nanometer technology analysis. For BSIM, the short-channel effect is included in the Vth computation as shown in:

\[ V_{th} = V_{th0} + K_1 \left( \sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s} \right) - K_2 V_{BS} + K_3 \left( 1 + \frac{Nlx}{L_{eff}} - 1 \right) \sqrt{\phi_s} - \Delta V_{th}. \]  

In the equation above, \( \Delta V_{th} \) is threshold voltage reduction due to the short channel effect and \( L_{eff} \) is effective channel length. \( K_1, K_2, \phi_s \), and \( Nlx \) are coefficients defined in the BSIM model.

2) EKV Model

The equation of the threshold voltage used in the EKV model is:

\[ V_{th} = V_{th0} + \Delta V_{SCE} + \gamma \sqrt{V'_S} - GAMMA \sqrt{PHI}. \]  

In this equation, \( GAMMA \) and \( PHI \) are related to the fundamental process parameters. \( \Delta V_{SCE} \) is a parameter used to describe reverse short channel effect. \( V'_S \) is inversely proportional to bulk-source voltage.

3) PSP Model

The threshold voltage in the PSP model uses the following equation:

\[ V_{th} = V_{FB} + P_D (V_{BS} + \phi_B + 2\phi_T) - V_{BS} + G \sqrt{\phi_B} (V_{BS} + \phi_B + 2\phi_T). \]  

In Eq. (4), \( V_{FB} \) is flat-band voltage and \( P_D \) is drain STI-edge perimeter. \( \phi_B \) and \( \phi_T \) are coefficients defined in the PSP model. \( G \) is used to describe bias dependent body factor.

According to (2)-(4), the three models all consider the impact from the bulk terminal voltage. When absolute value of \( V_{BS} \) increases, \( V_{th} \) will decrease. Since different parameters are used to describe the relationship between the threshold voltage and the bulk terminal voltage, performance of these models in the bulk-driven applications may be different from each other. In the EKV model, more parameters have been used to compute \( GAMMA \), \( PHI \), \( V_{th0} \), and \( \Delta V_{SCE} \). And this model also accounts for charge-sharing and reverse short-channel effects, which may be beneficial to bulk-driven applications.

3. Experimental Results and Analyses

In this section, comparison and analysis are discussed for 0.18μm and 90nm technologies. The model cards used for simulation are all extracted based on the corresponding technology.
3.1. For 0.18μm Technology

1) Gate-driven Configuration

Firstly, we conduct comparison and analyses of the gate-driven applications between simulation and measurement. Here, we analyze the relationship between the drain current and the gate-source voltage. The MOSFET channel size is 1.8μm for width and 0.18μm for length. The results are shown in Figure 1.

![Fig.1 Relationship of Drain Current and Gate-source Voltage with W=1.8μm and L=0.18μm. (a) NMOS (b) PMOS](image)

From these relationships between the drain current and the gate-source voltage, we can also find that the measurement curves lie among simulation results and have the same trends as others. In these figures, the measured drain currents are larger than zero when the gate-source voltage is less than the threshold voltage. This is because the impact of the ESD components placed in the fabricated devices has been included in the measurement.

2) Bulk-driven Configuration

The relationships of VBS-Id for NMOS and PMOS under the bulk-driven configuration are shown in Figure 2. In these figures, although the simulation results using the BSIM model cross the measurement curves, the simulation results with the EKV model show a closer trend with respect to the measurement results. Meanwhile, the curves of PSP show large deviation from others.

In Figure 2(a), the EKV and measurement curves have an increasing trend with similar gradients. However, the increasing gradient of the BSIM curve gets fairly flat when VBS reaches around 0V. The PSP model indicates about 20μA range in drain current when the channel width and length of the devices are 1.8μm and 0.18μm, respectively. The results in Figure 2(b) show a similar trend. An obvious deviation exists between the measurement curve and the simulation result using the PSP model, and drain currents experience large change when increasing voltage of bulk terminal. In addition, the EKV model shows a similar and closer curve to the measurement data than others.

<table>
<thead>
<tr>
<th>VBS</th>
<th>NMOS Vth (V)</th>
<th>PMOS Vth(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>M</td>
<td>B</td>
</tr>
<tr>
<td>0V</td>
<td>0.4</td>
<td>0.52</td>
</tr>
<tr>
<td>±0.5V</td>
<td>0.28</td>
<td>0.4</td>
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</table>

According to the results above, we also can see the difference in the amount of drain currents for the gate-driven and bulk-driven configurations. In the gate-driven configuration, for NMOS, the simulation and
measurement results achieve the drain currents of around 10\(\mu\)A when \(V_{GS} = 0.5\)V, whereas in the bulk-driven configuration, drain currents are around 30\(\mu\)A when the bulk-source voltage is only 0V. For PMOS, in the gate-driven configuration, the simulation and measurement results indicate that drain current is between 0\(\mu\)A and -5\(\mu\)A when gate-source voltage is -0.5V; but in the bulk-driven configuration, when bulk-source voltage is -0.5V, the drain current can reach around -30\(\mu\)A.

Obviously, the bulk-driven configuration is able to offer a higher drain current compared to the gate-driven configuration for the same input voltages. So if using the bulk-driven configuration, it is possible for a low input voltage to achieve a high current that can only be managed with a much higher input voltage in the gate-driven applications.

![Graph](image)

**Fig.2 Relationship of Drain Current and Bulk-source Voltage with \(W=1.8\mu m\) and \(L=0.18\mu m\). (a) NMOS (b) PMOS**

### 3) Threshold Voltage

Threshold voltage is an important parameter for MOSFET. One problem in the design of the modern low-voltage analog circuits is that the threshold voltage does not decrease as fast as the power supply along with the development of advanced technologies [4]. The reduction of threshold voltage under the bulk-driven configuration is normally expected from the theoretical point of view. Based on the simulation and measurement results, the threshold voltages for both NMOS and PMOS have been obtained and listed in Table 1. In this table, \(\pm 0.5\) means a positive voltage of 0.5V is imposed between the bulk and source terminals of NMOS and a negative voltage of -0.5V is used for PMOS.

According to Table 1, in the gate-driven configuration, when \(V_{BS} = 0\)V, the threshold voltages are about 0.4V for NMOS and -0.5V for PMOS. However, as for the bulk-driven configuration, when \(V_{BS} = \pm 0.5\)V, we can see that the threshold voltage is reduced due to the body effect. The simulation results using three models indicate the reduction in threshold voltage for both NMOS and PMOS, which conforms to the theoretical analysis for the bulk-driven configuration. Furthermore, for NMOS, the threshold voltage reduction of the BSIM model is 0.12V and that of the EKV model is 0.21V. But the threshold voltage reduction for the PSP model is only 0.04V. Similarly for PMOS, values from the BSIM and EKV models have larger change compared to that of the PSP model under the bulk-driven configuration. When compared with the measurement, the PSP model shows the closest estimation followed by the EKV model. The estimation reported by the BSIM model exhibits the largest deviation from the measurement results.

### 4) Transconductance

Transconductance (Gm) can be used as a measure of the sensitivity of drain current to any change in gate-source bias. When the channel size shrinks, many factors become variable and involve some uncertainties. To focus on the bulk-driven configuration, we analyze the relationship between Gmb
The transconductance in bulk terminal \((G_{mb})\) is shown in Figure 3.

As shown in the figures, compared to the measurement results, the \(G_{mb}\) from the EKV model under the bulk-driven configuration increases in a more similar manner than those from the BSIM and PSP models. For the BSIM model, when \(V_{BS}\) is greater than 0.35V for NMOS or less than -0.6V for PMOS, the increasing speed slows down and the curves become relatively flat. On the other hand, the PSP model exhibits a more sensitive relationship between \(G_{mb}\) and \(V_{BS}\) than the measurement result for PMOS.

![Fig. 3 Relationship of \(G_{mb}\) and Bulk-source Voltage with \(W=1.8\mu m\) and \(L=0.18\mu m\). (a) NMOS (b) PMOS](image)

### 3.2. For 90nm Technology

The EKV model card used for this paper is supported by the EKV research group. The model card version for 0.18\(\mu m\) is EKV2.6, however, for 90nm technology, the EKV model card version is 3. The PSP model for 90nm has been extracted based on NXP semiconductors 90nm technology. In this section, the comparison and analysis for 90nm technology are conducted among BSIM, EKV, PSP models and measurements. As the minimum width for 90nm technology is 0.1\(\mu m\), the chosen transistor size is 1\(\mu m\) for width and 0.1\(\mu m\) for length.

1) **Gate-driven Configuration**

With the same configuration, relationships between the drain current and the gate-source voltage are given for NMOS and PMOS in Figure 4.

According to Figure 4, simulation results from the measurement and EKV models are quite close although the curves based on the BSIM model is little close to the measurement for NMOS. However, big difference exits between measurement and BSIM model for PMOS When gate-source is 0.5V for NMOS and -0.5V for PMOS, the drain currents of the BSIM model are 16\(\mu A\) and -5\(\mu A\), compared to 60\(\mu A\) and -50\(\mu A\) for measurement and 80\(\mu A\) and -97\(\mu A\) for EKV models, respectively, however, for PSP model, the drain current value is 170\(\mu A\) and -148\(\mu A\) at this point.

2) **Bulk-driven Configuration**

The relationship between drain current and bulk-source voltage for 90nm technology is given in Figure 5. Figure 5 also shows that results using EKV model is more close to measurement data. Results from different models show large deviation from each other, but having a similar trend to measurement for NMOS. The average difference between measurement and EKV model is around 16\(\mu A\), 22\(\mu A\) for measurement with BSIM and 32\(\mu A\) for PSP with measurement. The highest drain current (ranging from 71\(\mu A\) to 134\(\mu A\)) is obtained from the PSP model, whereas a higher drain current (from 51\(\mu A\) to 99\(\mu A\)) is
computed from the EKV model; and a range from 35μA to 85μA is for measurement. For the BSIM model, the drain current is very low, only from 14μA to 60μA. A comparison among the three models exhibited for PMOS under the bulk-driven configuration shows the EKV model and measurement have large drain current, however BSIM and PSP has little drain current. Moreover, similar to the summary derived for the 0.18μm technology, Figures 4 and 5 indicate that larger drain currents can be offered from the bulk-driven MOSFETs compared to the gate-driven MOSFETs when input signals are the same.

3) Transconductance

Similar to the analyses for 0.18μm technology, Transconductance analyses for 90nm technology have been chosen. Figure 6 show the results for transconductance between bulk and source terminal based on 90nm technology respectively.

Figure 6 shows the relationship between Cbs and bulk-source voltage. Figure 6 (a) and (b) indicate the curves for EKV are obviously more close to measurement results than those of BSIM and PSP. In the figure 6, BSIM curves fluctuate slightly and are big different to measurement results. In figure 6(a), although PSP curve is close to measurement result when bulk-source voltage is less than 0.06v, its trend changes to falling when bulk-source voltage is greater than 0.06v.
3.3. Summary and Assessment of Distinct Models

Based on the comparison and analyses of simulation and measurement results, we can find that the bulk-driven technique shows obvious advantages over the traditional gate-driven scheme in low-voltage and low-power applications. When imposing small value of voltage on bulk terminal, relatively large drain current for the low-voltage and low-power circuit design can be obtained and the threshold voltage is reduced. Furthermore, the EKV model shows the best performance for submicron and nanometer bulk-drain applications.

4. Conclusions

In this paper, we measured MOSFET devices and run simulations with the BSIM, EKV, and PSP models in 0.18μm and 90nm technologies. Based on the experimental results, the bulk-driven technique shows obvious advantages over the traditional gate-driven scheme in low-voltage and low-power applications. The bulk-driven technique is capable of overcoming the bottleneck caused by the threshold voltage that cannot decrease at the same pace as the supply voltage of MOSFETs in the advanced technology. Furthermore, this promising technique does not require any modification of the existing MOSFET structure.

For submicron and nanometer technology, comparisons and analyses among measurement results and simulations with the BSIM, EKV, and PSP models have been made. It is found that the EKV model is the most suitable for the submicron and nanometer bulk-driven applications up to present main MOSFETs models.

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